**WHAT IS CLAIMED IS:**

1. A logarithmic transformer comprising:

a first bit string generator for generating a first bit string of binary data indicating the position of a highest order bit of logic "1" out of bits of digital data to be logarithmically transformed; and

a second bit string generator for determining, from said digital data, a second bit string of order lower than said highest order bit of logic "1",

the logarithmic transformer outputting logarithmic transformation data, which includes said first bit string as an integral part of a logarithmic transformation value resulting from a logarithmic transformation of said digital data and said second bit string as a fractional part of said logarithmic transformation value.

2. The logarithmic transformer according to claim 1, wherein said first bit string generator comprises:

a detecting unit for detecting the position of said highest order bit of logic "1" out of the bits of said digital data; and

a generating unit for generating said first bit string based on a result of detection by said detecting unit.

3. The logarithmic transformer according to claim 2, wherein

said detecting unit detects said highest order bit of logic "1" by decoding said digital data.

4. The logarithmic transformer according to claim 2, wherein said generating unit contains pieces of binary data indicating the positions of the respective bits of said digital data, and selects one out of said pieces of binary data based on the result of detection by said detecting unit, thereby generating said binary data indicating the position of said highest order bit of logic "1."

5. The logarithmic transformer according to claim 4, wherein said generating unit is composed of a switching circuit for selecting one out of said pieces of binary data, based on the result of detection by said detecting unit.

6. The logarithmic transformer according to claim 2, wherein said detecting unit comprises:

a first logic circuit for outputting data for excluding a bit string lower than said highest order bit of logic "1" from the bits of said digital data; and

a second logic circuit for removing the bit string excluded by said data from the bits of said digital data, thereby detecting said highest order bit of logic "1."

7. The logarithmic transformer according to claim 6, wherein:

said first logic circuit includes a plurality of OR gates for inputting respective bits of said digital data from a most significant bit to a least significant bit, said OR gates having their outputs and inputs cascaded in association with the most significant bit

to the least significant bit; and

said OR gates generate said data for excluding by performing OR operations between the outputs of said OR gates of higher order bits and the respective bits of said digital data.

8. The logarithmic transformer according to claim 6, wherein

said second logic circuit detects said highest order bit of logic "1" by performing AND operations between the respective bits of said digital data and said data for excluding.

9. The logarithmic transformer according to claim 1, wherein

said second bit string generator determines, as said second bit string, a bit string of a predetermined number of bits including a bit following said highest order bit of logic "1" out of the bits of said digital data.

10. The logarithmic transformer according to claim 9, wherein

when the number of bits from the bit following said highest order bit to a least significant bit of said digital data falls short of said predetermined number, said second bit string generator appends as many bits as a shortfall to the least significant bit to generate, as said second bit string, a bit string of said predetermined number of bits.

11. The logarithmic transformer according to claim 9, wherein said second bit string generator comprises:

a second bit string extracting unit for inputting said digital

data as successive bit strings each having said predetermined number of bits; and

a second bit string selecting unit for making said second bit string extracting unit to extract, as said second bit string, a bit string of said predetermined number of bits having the bit following said highest order bit of logic "1" as a most significant bit of said bit string of said predetermined number.

12. The logarithmic transformer according to claim 11, wherein said second bit string selecting unit detects said highest order bit of logic "1" by decoding said digital data.

13. The logarithmic transformer according to claim 12, wherein said second bit string extracting unit extracts the bit string of said predetermined number of bits including the bit following said highest order bit as the most significant bit, based on the result of detection decoded by said second bit string selecting unit.

14. The logarithmic transformer according to claim 11, wherein said second bit string extracting unit is composed of a switching circuit for extracting the bit string of said predetermined number of bits based on the result of detection by said second bit string selecting unit.

15. A method of logarithmic transformation comprising:

a first bit string generating step of generating a first bit

string of binary data indicating the position of a highest order bit of logic "1" out of bits of digital data to be logarithmically transformed; and

a second bit string generating step of determining, from said digital data, a second bit string of order lower than said highest order bit of logic "1",

wherein logarithmic transformation data on said digital data is generated by using said first bit string as an integral part of a logarithmic transformation value resulting from a logarithmic transformation of said digital data and said second bit string as a fractional part of said logarithmic transformation value.